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U.S. PTO

**PLANT PATENT APPLICATION TRANSMITTAL**  
**(Only for new nonprovisional applications under 37 CFR 1.53(b))**

223390 U.S. PTO  
10/811241

032504

Docket No. : 52182/DBP/A400  
Inventor(s) : Kazunari Iwaki; Takuro Ishihara; and Shinya Miyano  
Title : PETUNIA PLANT NAMED 'SUNPATIKI'  
Express Mail Label No. : EV327880828US

**ADDRESS TO:** Commissioner for Patents  
Mail Stop Patent Application  
P.O. Box 1450  
Alexandria, VA 22313-1450

Date: March 25, 2004

1.  **Fee Transmittal Form** (*Submit an original and a duplicate for fee processing*)

2. **Application Comprised of**

8 Specification, Claim and Abstract  
2 x  2 sheets color drawing(s) (2 copies required of each view - 37 CFR 1.165(b))

**Declaration and Power of Attorney**

Newly executed (original or copy)  
 Unexecuted declaration

3. **Applicant(s) Status Under 37 CFR § 1.27**

Applicant(s) and any others associated with it/them under § 1.27(a) are a SMALL ENTITY

4. **Also Enclosed are**

Plant Color Coding Sheet  
 Preliminary Amendment  
 An Assignment with the Recordation Cover Sheet and the recordation fee are enclosed as separate papers  
 37 CFR 3.73(b) Statement (when there is an assignee)  
 Information Disclosure Statement (IDS)/PTO/SB/08A/B  
 Copies of citations  
 Certified Copy of Priority Document(s) (*if foreign priority is claimed*)  
 English Translation Document (*if applicable*)  
 Return Receipt Postcard (MPEP 503) (should be specifically itemized)  
 Other

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**5. CORRESPONDENCE ADDRESS**

***CHRISTIE, PARKER & HALE, LLP, P.O. BOX 7068, PASADENA, CA 91109-7068***  
**Customer Number: 23363**

Respectfully submitted,  
CHRISTIE, PARKER & HALE, LLP

By *D. Bruce Prout*  
D. Bruce Prout  
Reg. No. 20,958  
626/795-9900

DBP/aam

**FEE TRANSMITTAL  
PLANT PATENT APPLICATION**

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**FILING FEE**

Applicant Status: Applicant(s) is/are a **large** entity.

**METHOD OF PAYMENT**

No filing fee enclosed.

No Deposit Account Authorization.

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

By   
D. Bruce Prout  
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626/795-9900

DBP/aam  
AAM PAS557099.1-\* 03/25/04 11:22 AM

combining Eranian and Gillies is improper, and showing a *prima facie* case of obviousness fails.

For the foregoing reasons, claim 1 is patentable. Claims 2-5 depend from claim 1, and are therefore patentable for at least the same reasons as claim 1. Claims 2-5 are also patentable for their additional limitations.

Regarding claim 3 with the further limitation “modifying the number O of the first parameters to generate the number O of the second parameters,” the Office Action cited Figure 5 and *asserted without explaining* “outputs from function A and combined output from B.” Those skilled in the art will recognize that alloc . . . 5, 4, 0, 0 of Eranian indicates that *zero* register is to be allocated for the output registers. This is evidenced by the fact that only input and local registers, but *no output registers*, are shown associated with the B: alloc statement. Further, there is nothing in Eranian that indicates modifying the *number O (of output register)* of the first parameters to generate the number O of output registers of the second parameters. Additionally, as indicated above, there is no first statement and no first parameters in Eranian, there cannot be modifying the first number O of output registers used in the first statement.

Regarding claim 4, the Office Action asserted “function A call *output parameters* r47-r52 matching with *Input parameters* r32-r36 of the Output of the B call is equivalent to using the O of the first parameters, while r37-r41 in B output is the equivalent of N from the 1<sup>st</sup> parameters so that O from B is the combined O and N from the 1<sup>st</sup> parameter.” It is respectfully submitted that the recitation of claim 4 is not about “using the O of the first parameters” or using output parameters as Input parameter as cited by the Office Action. Rather, reading in conjunction with claim 1 and 2, claim 4 recites using the *number O of output registers* of the first parameters in generating *the number O of output registers* of the second parameters. In the

illustrative embodiment of FIG. 4, the number O of output registers of the first parameters is 2 while the number O of output registers of the second parameters is 6, and N equals to 4, which indicates that 4 registers is to be allocated. Additionally, the number N (or 4 in the illustrative embodiment) is not “from the 1<sup>st</sup> parameters,” as asserted by the Office Action. In fact, the number N is the number of registers to be allocated. Further, as indicated above with regards to claim 3, there is no first statement and no first parameters in Eranian, and, as a result, there cannot be using the number O of output registers of the first parameter as inputs in generating the number O of the second parameter. Further, as also explained in connection with claim 3, in Eranian, *zero* number of output registers is to be allocated from the statement alloc . . . 5, 4, 0, 0, and there is no indication that this zero number of output registers to be allocated is a result of using the N (or 4) of registers to be allocated and the number O of output registers of the first parameters used in the first statement.

Explanation with respect to claim 4 is applicable to claim 5. Further, as indicated, the number O of output registers in the B: alloc statement is *zero* (alloc 5, 4, 0, 0), and there is no indication that this *zero equals* the number N of registers to be allocated and the number O of output registers of the fist parameters used in the first statement.

Therefore, claims 3-5 are patentable for their additional limitations.

Claims 6-10 and 11-15 recite limitations corresponding to claims 1-5, and are therefore patentable for at least the same reasons as claims 1-5.

**SUMMARY**

In conclusion, it is submitted that pending claims clearly present subject matter that is patentable over the prior art of record, and withdrawal of the rejections is respectfully solicited.

Respectfully submitted,

Date: 1/10/05 By: Tuan V. Ngo  
Tuan V. Ngo, Reg. No. 44,259  
IP Administration  
Legal Department, M/S 35  
Hewlett-Packard Company  
P. O. Box 272400  
Fort Collins, CO 80527-2400  
Phone (408) 447-8133  
Fax (408) 447-0854